REMARKS

Claim Rejections – 35 U.S.C. §103

Applicant would like to bring to Examiner's attention the fact that Claims 8, 9, 17, 18, 26, 27, 35, and 36 were previously held to be allowable by Examiner. On Page 12 of the Office Action dated June 6, 2005 and Pages 13-14 of the Office Action dated December 17, 2004, Examiner provided reasons for the allowance of Claims 8-9, 17-18, 26-27, and 35-36, stating, "The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims. For instance, Shinohara et al. (US 2004/0000681 A1) teach the claimed transistor structure but falls to teach the substrate, p-type region and the p-type buried layers each biased such that the p-type region is fully depleted. Masamichi (JP 61123171 A) teaches each of the n-type buried layers being biased but fails to teach biasing the other regions, a fully depleted region and the claimed transistor structure. Lee (US 6,329,246 B1) teaches biasing the other regions but fails to teach biasing each of the buried layers and a fully depleted region. And Ohsawa (US 2004/0026749 A1) teaches a fully depleted p-type region but fails to teach the claimed biased layers. The dependent claims being further limiting and definite are also allowable."

Examiner seems to have withdrawn the previous allowance of claims based on a new search. According to MPEP 76.04, "an examiner should not take an entirely new approach or attempt to reorient the point of view of a previous examiner, or make a new search in the mere hope of finding something."

Therefore, in light of Examiner's previous allowance of Claims 8, 9, 17, 18, 26, 27, 35, and 36, Applicant respectfully requests that Examiner reconsider and withdraw the present rejection of Claims 8, 9, 17, 18, 26, 27, 35, and 36.

Claims 8-9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Williams et al. (US 5,726,477).

For a §103 obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. MPEP 2143.

Claim 8 recites a transistor for an integrated circuit comprising "a p-type substrate; an n-type region disposed over said p-type substrate; n-type buried layers disposed at about a boundary between said substrate and said n-type region, said buried layers doped to a higher level than said n-type region ... said substrate, said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted."

Applicant respectfully submits that Williams fails to disclose the substrate, the n-type region and the n-type buried layers each biased such that the n-type region is fully depleted, as recited in Claim 8. In fact, on Page 3 of the Office Action dated November 21, 2005, Examiner even admits that Williams fails to teach "said substrate and said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted."

Examiner argues that it would have been obvious to one having ordinary skill in the art at the time the invention was made to also bias the n-type buried layers of the transistor structure as taught by Williams et al. so that the n-type region is fully depleted

to create threshold adjustable transistors. Examiner cites Col. 2, lines 50-55 of Williams as disclosing this motivation. However, this passage merely discusses a need "for a technique for adjusting the V_t of MOSFET devices in processes that allow fabrication of mixed device types, while preserving the ability to use long diffusion and high temperature steps subsequent to polysilicon gate deposition." There is no discussion in Williams of biasing the substrate, the n-type region and the n-type buried layers such that the n-type region is fully depleted, or how this limitation is related to the motivation mentioned above.

Applicant respectfully submits that Examiner has not provided any evidence of this limitation being disclosed in the prior art. As stated in MPEP 2144.03(A), it "is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based." It is respectfully requested that evidence be provided, if possibly citable from the prior art, to prove that the prior art teaches all of the limitations of Claim 8, including the substrate, the n-type region and the n-type buried layers each biased such that the n-type region is fully depleted, or the rejection must be withdrawn. Broad conclusory statements standing alone are not evidence. MPEP 2144.03(C).

Applicant respectfully submits that Examiner has failed to establish that all elements of Claim 8 are disclosed in the prior art. Therefore, Applicant respectfully submits that Claim 8 is non-obvious over Williams and is currently in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

Since Claim 9 depends from Claim 8, Applicant respectfully submits that Claim 9 is also patentable as it contains the same limitations as Claim 8.

Furthermore, Claim 9 recites the transistor of claim 8 further including "an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate."

Williams fails to disclose an isolation trench *extending down into* the substrate, as recited in Claim 9. On Page 3 of the Office Action dated November 21, 2005, Examiner cites FIG. 12, Col. 9, lines 1-67 and Col. 10, lines 1-59 as teaching isolation regions 406 and 408 extending down into the substrate 402. However, FIG. 12 only shows isolation regions 406 and 408 disposed *next to* substrate 402. Regions 406 and 408 clearly do not extend *down into* the substrate. Applicant cannot find, nor has Examiner cited, any disclosure in Williams of an isolation trench *extending down into* the substrate, as recited in Claim 8.

Since Williams fails to teach this limitation, Applicant respectfully submits that Examiner has failed to establish that all elements of Claim 9 are disclosed in the prior art. Therefore, Applicant respectfully submits that Claim 9 is non-obvious over Williams and is currently in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 26-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Williams, and further in view of Uchida (US 2002/0031882 A1).

Applicant respectfully submits that the same arguments made above with respect to the patentability of Claims 8 and 9 are also applicable to the patentability of Claim 26 and 27, respectively.

Furthermore, since Claim 27 depends from Claim 26, Applicant respectfully submits that Claim 27 is also patentable as it contains the same limitations as Claim 26. Additionally, although Examiner cites FIG. 5 in arguing that Uchida teaches an isolation

trench 2 disposed in the p-type region and surrounding the source and drain regions, trench 2 clearly does not extend *down into the substrate*, as recited in Claim 27.

Therefore, Applicant respectfully submits that Claims 26-27 are currently in condition for allowance as they are non-obvious over Williams in view of Uchida. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 17-18 and 35-36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Williams and Uchida, and further in view of Taniguchi et al. (US 6,617,632 B2).

Applicant respectfully submits that the same arguments made above with respect to the patentability of Claims 8-9 and 26-27 are applicable to the patentability of Claims 17-18 and 35-36 as well.

Furthermore, since Claims 18 and 36 depend from Claims 17 and 35 respectively, Applicant respectfully submits that Claims 18 and 36 are also patentable as they contain the same limitations as their respective parent claims.

Therefore, Applicant respectfully submits that Claims 17-18 and 35-36 are currently in condition for allowance as they are non-obvious over Williams and Uchida in view of Taniguchi. Reconsideration and withdrawal of the rejection is respectfully requested.

If the Examiner has any questions regarding this application or this response, the Examiner is requested to telephone the undersigned at 775-586-9500.

Respectfully submitted,
SIERRA PATENT GROUP, LTD.

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Jonathan D. Hanish
Reg. No.: 57,821

Sierra Patent Group, Ltd.
1657 Hwy. 395, Suite 202
Minden, NV 89423
(775) 586-9500
(775) 586-9550 Fax